IN THE CLAIMS

Claims 1-9 (Canceled).

10. (Currently Amended) An integrated circuit comprising:

a semiconductor structure;

a first trench formed of a first depth in said semiconductor structure;

a temporary covering on said first trench and over said semiconductor structure, said temporary covering being thicker in said first trench than over said semiconductor structure; and

said temporary covering having an opening through a thinner portion of said temporary covering that is over said semiconductor structure, said thinner portion other than the thicker temporary covering in said first trench, said opening to define a region for a second trench.

11. (Currently Amended) The circuit of claim 10 wherein said temporary covering is spin-on glass.

Claims 12-15 (Canceled).

16. (Previously Presented) The circuit of claim 10 wherein said opening is a second trench.

17. (Previously Presented) The circuit of claim 16 wherein said second trench extends transversely to said first trench.

18. (Previously Presented) The circuit of claim 17 wherein said second trench is shallower than said first trench.

19. (Currently Amended) The circuit of claim 10 wherein said opening does not extend through said ~~thicker~~ temporary covering in said first trench to expose said semiconductor structure.

20. (Currently Amended) The circuit of claim [[16]] 18 wherein said temporary covering in said first trench has an upstanding portion that extends beyond a bottom surface of said second trench.

21. (Previously Presented) An integrated circuit comprising:

a semiconductor structure;

a first and a second trench formed in said semiconductor structure, said first trench formed to a first depth, said second trench transverse to said first trench and formed to a second depth less than said first depth; and

a covering in said first trench and over said semiconductor structure, said covering having an opening therethrough, said opening in communication with said second trench.

22. (Previously Presented) The circuit of claim 21 wherein the covering partially fills said first trench.

23. (Currently Amended) [[the]] The circuit of claim 22 wherein the covering in said first trench includes an upstanding portion at the intersection of said first and second trenches, the upstanding portion extending above a bottom surface of said second trench to an upper surface of said substrate.

24. (New) The circuit of claim 21 wherein said covering is a temporary covering.

25. (New) The circuit of claim 21 wherein the portion of said covering that is over said semiconductor structure is thinner than a portion of said covering in said first trench, said thinner portion of said covering other than in said first trench.

26. (New) The circuit of claim 10 wherein said thinner portion of said temporary covering is over said semiconductor structure other than over said semiconductor structure in said trench.